PHASE LOCKED LOOP

1. Objectives

We will study the elements making up a Phase locked Loop and also one of its application: the PLL frequency synthesis.

2. Devices to study

The CMOS IC 4046 includes all the elements needed for a PLL,, except of the passives resistors and capacitors for the VCO and the loop filter.

We will study :

- The XOR phase detector (PD1).
- The sequential phase/frequency detector with three state output (PD2).
- The RC Voltage Controlled Oscillator (VCO).
- The Low-Pass loop filter.
- The closed Phase Locked Loop.
- The frequency multiplying with PLL synthesis.

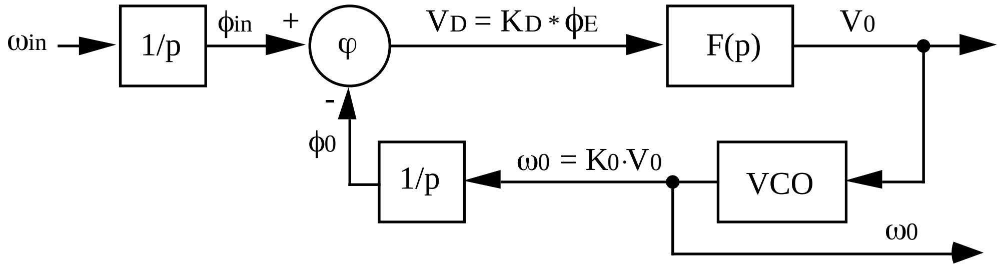
3. Bibliography

[1] Circuits et Systèmes Electroniques, Prof. M. Declercq

[2] Data sheets of HEF4046 & MC14046 en appendix

[3] Boucles à verrouillage de phase, M. Girard, éd. McGraw-Hill. Extrait en annexe

4. Block diagram of a PLL

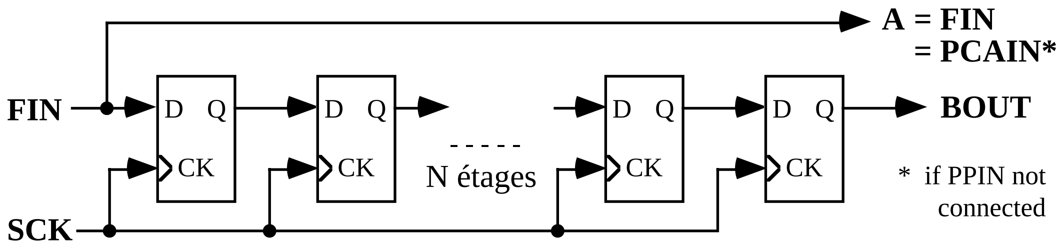


5. Phase detector

IC 4046 includes two different phase detectors[1]. Phase detector 1 is a simple XOR logic gate. Phase detector 2 is an asynchronous sequential logic circuit triggered by the rising edges at its inputs which is able to cover a range from -2π to $+2\pi$.

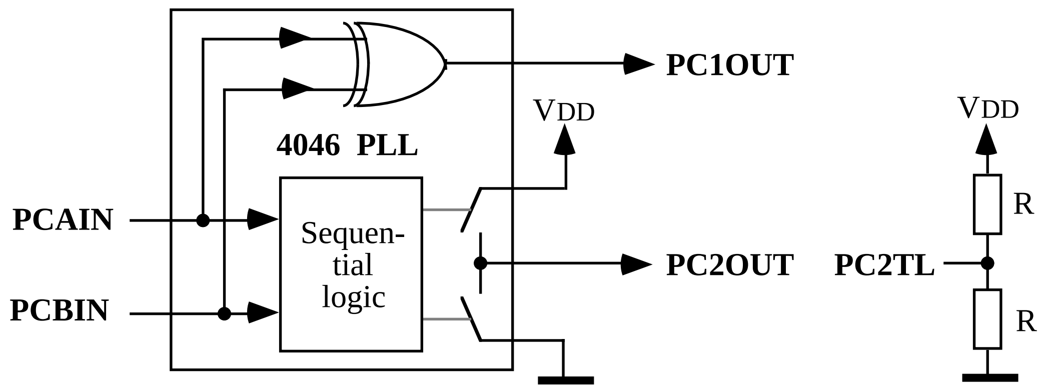
5.1 Variable phase shifter

To measure the characteristics of the sequential phase detector 2, a variable phase shifter covering à range of 4π without any discontinuity is needed. The following circuit is able to do it..



With a Nbit shift register (in this case N = 256), a binary input signal at fixed frequency f_{in} and a shift clock at $f_{CK} = N \cdot f_{in}/2$, output signal B is equal of signal A with a delay of two periods, so A and B are in phase. If f_{CK} is variable from $N \cdot f_{in}$ to $N \cdot f_{in}/3$, phase between A and B changes from -2π to $+2\pi$. However, as signal A and shift clock are not synchronous, the shifter generates a phase jitter of $\Delta ø = 2\pi f_{in}/f_{CK}$.

5.2 Phase comparators of the IC 4046



The temporary connection of PC2OUT with PC2TL is only a trick to measure the characteristics of PD2, by giving an output voltage of $V_{DD}/2$ when the output is in high Z state.

5.3 Data

- Phase comparators : PC1 & PC2 of HEF4046 with V_{DD} = 5 V
- R = 10 kΩ
- Signal FIN : binary 0 - 5 V, f_{in} = 1250 Hz, cyclic ratio = 50%

5.4 Theoretical forecasts

5.4.1 Draw signals PCAIN, PCBIN, PC1OUT et PC2OUT for various phase angles $\phi_E = \pm n\pi/4$ (n = 0, 1, 2, 3, 4). In each case, calculate the mean output voltage $\overline{V_0}$.

5.4.2 Draw the curve $\overline{V_0} = f(\phi_E)$ for $-2\pi \leq \phi_E \leq +2\pi$.

5.4.3 What is the effect of the cyclic ratio of PCAIN and PCBIN signals ?

5.5 Measurements

5.5.1 observe with a scope the output of both phase comparators for ϕ_E variable from -3π to $+3\pi$.

5.5.2 measure the mean output voltage and draw the characteristics $\overline{V_0} = f(\phi_E)$ of both phase comparators.

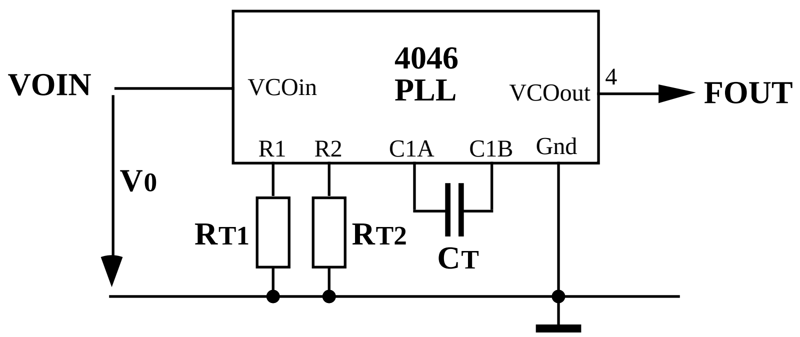
5.5.3 calculate the "gain" K_D of both phase detectors.

5.5.4 Observe the output signals and measure the mean voltage when input signals FIN=PCAIN and PCBIN are at slight different frequencies. Comment.

6. TheVoltage Controlled Oscillator

The VCO in the 4046 is an astable multivibrator. Its frequency is given by the input voltage VCOin, two resistors and a capacitor..

6.1 Principle schematics



6.2 Data

- VCO: VCO in CMOS HEF4046 with V_{DD} = 5 V
- f_0 = 10 kHz
- $\Delta f = \pm$ 4 kHz above and below f_0

6.3 Theoretical forecasts

6.3.1 using the data sheets of HEF4046, estimate R_1, R_2 and C for the given center frequency and span.

6.4 Measurements

6.4.1 Place the calculated elements in places R_{T1}, R_{T2}, C_T.

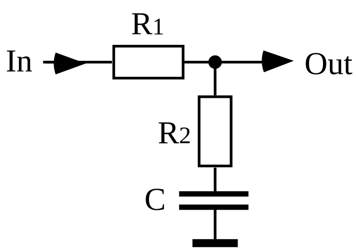
6.4.2 Apply an input voltage VOIN from 0 to 5 V and measure the output frequency FOUT. If necessary, modify R_{T1} and R_{T2} to cover the desired frequency range. Draw the characteristics $f_{out} = f(V_o)$. Comment.

6.4.3 Calculate the VCO "gain" K_0.

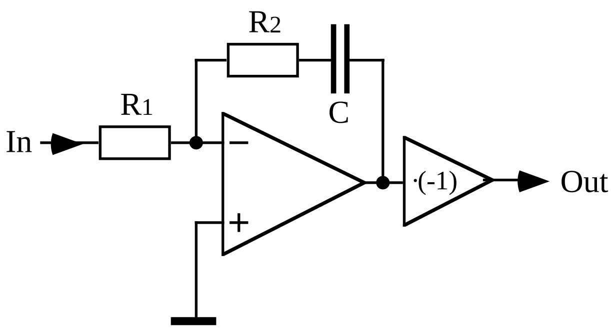
7. The Low-Pass loop filter

Simple PLL are of second order, using a loop filter of first order.

7.1 Principle schematics



Filter 1



Filter 2

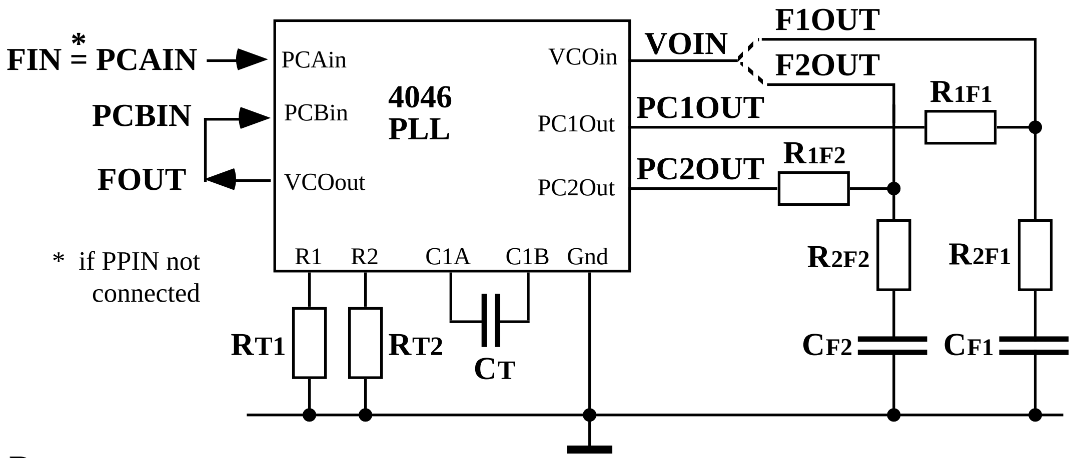
7.2 Theoretical study

7.2.1 Give the analytical expression of the transfer function and draw the bode plot for these two filters

8. Closed loop behaviour

Study of the stability, the transitory response, the capture and lock ranges of the closed phase locked loop.

8.1 Principle schematics of the PLL using the 4046 IC



8.2 Data

- PLL : IC CMOS HEF4046 with V_{DD} = 5 V

- FIN : binary signal 0 - 5 V 6 kHz ≤ fin ≤ 14 kHz cyclic ratio = 50%

- PLL Bandwidth : Bn = 500 Hz

- Quality factor : Q = 1

8.3 Theoretical forecast

8.3.1 The PLL using phase Comparator 1 and the passive filter 1 has actually the behaviour described in the application notes of MC14046.

The PLL using Phase Comparator 2, with its three state output connected to the passive filter 1, has in reality the behaviour of a PLL using filter 2, with an integrator in the loop (see ref [3]).

8.3.2 Calculate the elements of both filters to have the required bandwidth and damping with both phase comparators.

8.4 Measurements

Do the same measurements with both phase comparators with its associated filter.

To minimise disturbance of the loop by discharging C_{F2}, use a high impedance probe when measuring V_O on F2OUT.

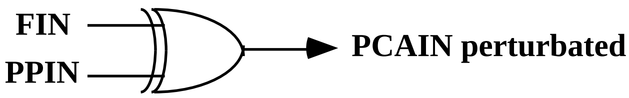
8.4.1 While changing f_{in}, observe the signals at the phase comparators inputs. Look at the phase difference. Observe also V_O. Commenter.

8.4.2 Measure the capture and lock ranges. Comment.

8.4.3 To study the response to a frequency step, modulate f_{in} with a low frequency square signal, using FM capability of the generator. Frequency step Δf_{in} must stay in the lock range. Observe signal V_0 for various Δf_{in}. Commenter.

8.4.4 Try to lock the PLL on an integer multiple or an integer divide of the specified f_{in}. Comment.

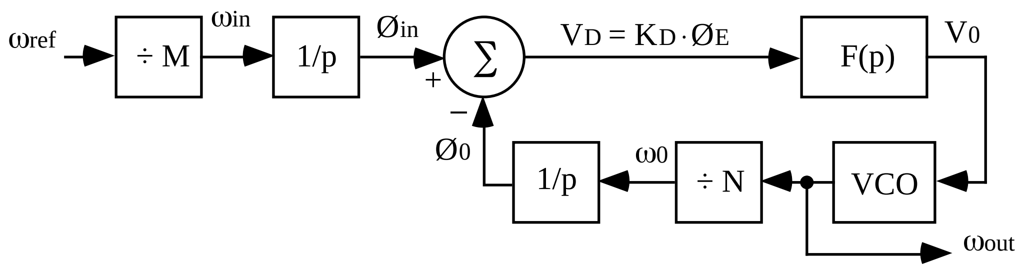
8.4.5 With the circuit draw bellow, wired on the experimentation board, add short perturbing pulses not correlated to the reference input signal. Study the response of the PLL to this noise.



When PPIN is leaved unconnected, a "pull-down" resistor makes PPIN = 0 and so PCAIN = FIN

9. Application : Frequency multiply by PLL synthesis

Frequency multiply or frequency synthesis is a common application of the PLL. There are many solution, but all based on the following basic principle.

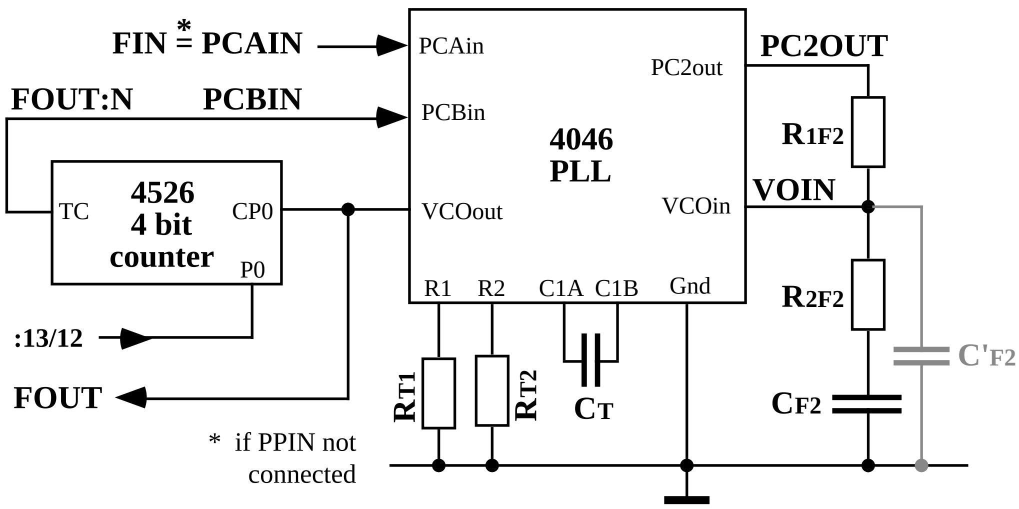


When the loop is locked and stabilised:

$$\omega_0 = \omega_{in} \quad \Rightarrow \quad \frac{\omega_{out}}{N} = \frac{\omega_{ref}}{M} \quad \Rightarrow \quad \omega_{out} = \frac{N}{M}\,\omega_{ref}$$

Compared with the simple PLL already studied, the only change is the dividing factor N introduced in the loop, which must be included in the K_O factor. The behaviour of the loop is function of N which is variable.

9.1 Principle schematics of the experimental circuit



The optional capacitor C_{F2} allows to add a second pole to the filter's transfer function, making a third order loop.

9.2 Data

- PLL : IC CMOS HEF4046 with V_{DD} = 5 V
- FIN = f_{ref} = 10 kHz
- M = 1
- N = 12 or 13 (4 Bit Binary Programmable Down Counter 4526)
- $Q \approx Q_{optimum}$
- Settling time : $t_s \approx$ 5 ms

9.3 Theoretical forecasts

9.3.1 Find the elements of the VCO (R_{T1}, R_{T2} and C_T) to obtain the desired output frequency. Take a large safety margin for the lock range. Make a quick measure of the VCO transfer curve to calculate its "gain". Calculate the elements of the loop filter to satisfy the settling time and damping requirements.

9.4 Measurements

9.4.1 To minimise disturbance of the loop by discharging C_{F2}, use a high impedance probe when measuring V_O on F2OUT.
For the different values of N, observe the signals at the phase comparators inputs. Look at the phase difference. Observe also V_O. Commenter.

9.4.2 Measure the settling time when changing N.

9.4.3 Observe the spectrum of the output signal around f_O. Commenter.

9.4.4 Propose a solution to improve spectral purity of the output signal. Experiment and comment.