

A/N & N/A CONVERTERS

1. Objectives

The goal of this work is to understand the operation of the A/N and N/A converters, to measure their precision and to familiarize with their implementation. One will study also problems involved in sampling and with the numerical processing of analogue signals.

2. Devices to study

- Integrated 8 bits A/N Converter ADC0820 (Philips or National Semiconductor), semi-flash switched capacitors with sample-hold
- Integrated 8 bits N/A Converter AD7524 (Analog Devices) based on the R-2R scale.
- Study of a numerical acoustic echo room .

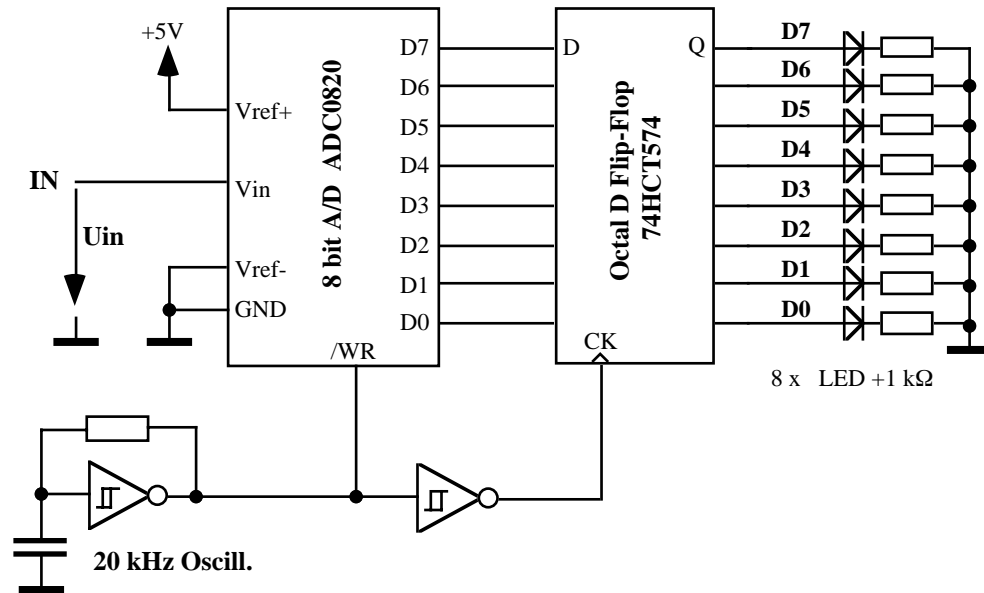
The assemblies are already carried out on printed circuit. The schematics are in appendix with this data.

3. Bibliography

- [1] Circuits et systèmes électroniques II , Prof. M. Declercq.
- [2] Schematics of the "D/A - A/D Experimentation Board" in appendix.
- [3] Schematics of the " chambre d'écho " in appendix.
- [4] Data Sheets on the intranet.

Master 1^{er} semestre**4. A/D Converter ADC0820**

The CMOS IC ADC0820 is a 8 bits semi-flash A/N converter, with 1 μ s conversion time.

4.1 Simplified schematics

IC ADC0820 has an internal sample-hold. It is not necessary in this first part, since we will make static measurements. On the other hand, it will be useful in part 6 for dynamic measurements.

The eight D flip-flop maintain value of the data provided by the A/N converter at the end of each conversion. An RC oscillator gives the sampling rate. An array of 8 LEDs makes it possible to visualize the state of the bits at the output.

4.2 Data

- Input range: 0 to +5 V.
- Reference voltage : +5 V.
Supply voltage is used as reference. Check its accuracy and stability.
- Resolution : 8 bits.
- Sampling frequency : 20 kHz.

Master 1^{er} semestre**4.3 Theoretical forecasts**

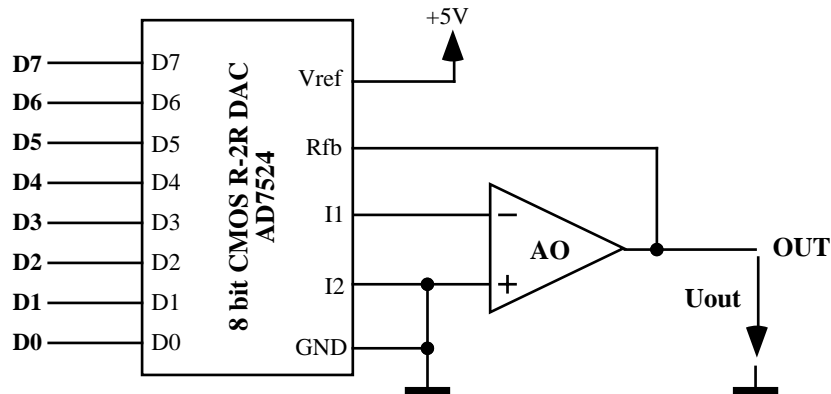
- 4.3.1 Give a short explanation of how a semi-flash ADC works.
- 4.3.2 Calculate the input voltages corresponding to the transition between successive output numbers 0 to 6, de 121 to 135 and 250 to 255.

4.4 Measurements

- 4.4.1 Adjust power supply at 5.000 V.
- 4.4.2 Apply a variable input voltage and measure the values corresponding to the transition between successive output numbers 0 to 6, de 121 to 135 and 250 to 255.
- 4.4.3 Plot the transfer curve between output codes 121 to 135. Comments ?.

Master 1^{er} semestre**5. D/A Converter AD7524**

The IC AD7524 is a 8 bit N/A converter using R/2R ladder. An external op amp gives a voltage output.

5.1 Simplified schematics

On the PCB each bit line is connected to a pull-down resistor et which gives a low logic level to an unconnected input. To give a high logic level connect the input to the "1" pin \Leftrightarrow +5V..

5.2 Data

- Reference voltage : +5 V.
Supply voltage is used as reference. Check its accuracy and stability.
- Resolution : 8 bits.

5.3 Theoretical forecasts

- 5.3.1 Give a short description of how this type of DAC works.
- 5.3.2 Calculate the voltage step corresponding to each input bit.
- 5.3.3 Calculate the output voltage corresponding to the two input state 00000000 and 11111111.

5.4 Measurements

- 5.4.1 Adjust the power supply voltage at 5.000 V.
- 5.4.2 Measure the voltage step corresponding to each input bit. Conclude on the monotonicity.
- 5.4.3 Measure the output voltage corresponding to the two input state 00000000 and 11111111.. Calculate the offset and gain error.

Master 1^{er} semestre**6. Complete processing A/N + N/A**

By cascading the ADC and the DAC, one should theoretically recover at the output the input signal with quantization noise.

6.1 Circuit description

Connecting each output bit of the ADC to the corresponding input bit of the DAC should give: $U_{out} = -U_{in}$.

The ERR output give $-(U_{in}+U_{out})$ which is a measure of the error during the global signal processing.

6.2 Data

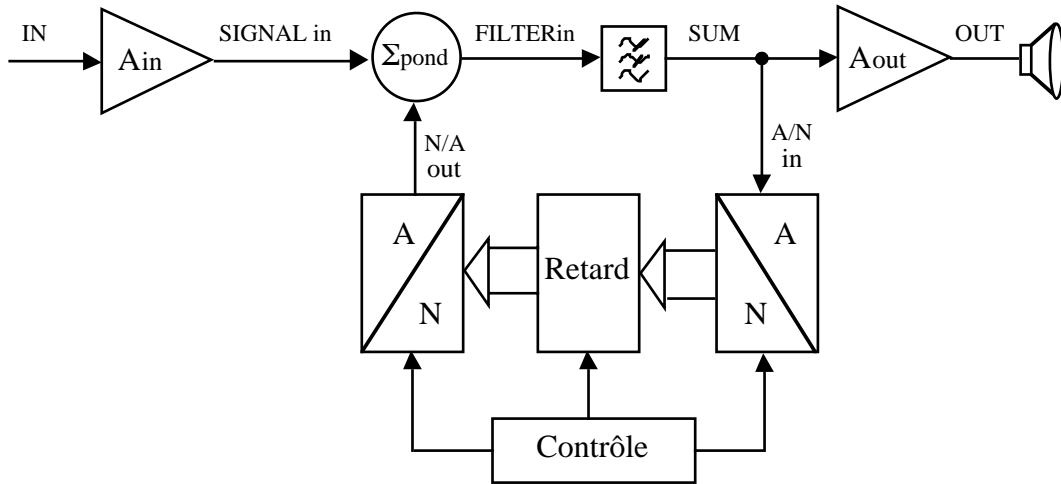
- Input range: 0 to +5 V.
- Reference voltage : +5 V.
Supply voltage is used as reference. Check its accuracy and stability.
- Resolution : 8 bits.
- Sampling frequency : 20 kHz.

6.4 Measurements

- 6.4.1 With a triangular signal at the input, observe and comment the errors created by the signal processing.
- 6.4.2 With a pure sinusoidal waveform at the input, measure the spectrum of the output signal. Show the result of the sampling.

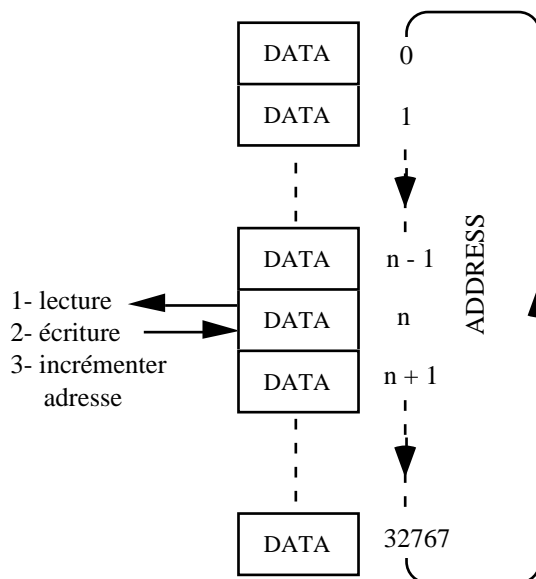
7. Application : an echo room.

7.1 Principle



Delaying a numerical signal is made by passing it in a FIFO register made in RAM. This RAM can be addressed by two methods:

- a. at fixed sampling frequency with adjustable register depth.
- b. at adjustable sampling frequency with a fixed register depth, which is made by a circular buffer in RAM. At each successive address generated by a binary counter, we read the old DATA the write a new one. Delay equals one complete scan of the RAM.



7.2 Circuit description (see schematics in appendix)

A two stage amplifier with adjustable gain at the second stage, rises voltage level to match the ADC input range. The delayed signal (echo) is added to the

Master 1^{er} semestre

direct signal. A low-pass filter makes pre and post filtering, because it is placed before the ADC and after the DAC. A simple state machine controls the operations Read Write and Increment address. A final audio power amplifier drives the speaker.

7.3 Datas

- Memory size : 32'768 Bytes
- Sampling frequency : $f_s = 2$ to 600 kHz, adjustable through the Δt pot on the front panel and by selecting one of the output of a clock divider. The delay is adjustable from 0.05 s to 16 s ,but Niquist limit is not correct on the hole range.
- Audio bandwidth : 15 kHz.
- Standard positions of the switches are: SW1: Audio in, SW2: SIGNAL in on, SW3: ECHO on, SW4: SUM et SW5: HP on. One must connect SELECT CK to CLK.

7.4 Theoretical forecasts

- 7.4.1 How much should be the attenuation of the echo signal .
- 7.4.2 What is the maximum delay achievable complying with the audio bandwidth.
- 7.4.3 Calculate min an max values of the input amplfier's gain.
- 7.4.4 Draw the control signals CLK, CK, /CK, INC, R/W and the corresponding data on the bus.

Master 1^{er} semestre**7.5 Measurements**

- 7.5.1 Apply different signals at the input (pure sinus, speech, music) and try the different possible configurations
- 7.5.2 With the dipswitches modify the number of bit of the numerical processing, and comment the audio quality.